REMARKS

The claims of the present application are subject to a restriction requirement, and in a telephone conference with the Examiner on February 2, 2005, Group I (claims 1-4 and 9-15) was elected for prosecution in this application. Applicant hereby confirms the election. Applicant expressly reserves the right to file claims relating to the non-elected invention in a divisional application.

Drawings

Applicant submits herewith a replacement drawing sheet containing an amended Figure 2. Figure 2 has been amended to include reference number "40".

Claims

In the Office Action, the Examiner rejected claims 9 and 13 under 35 U.S.C. §112, asserting that the disclosure is non-enabling. The Examiner is unclear where the "time data" comes from.

Basically, there is no "time data" per se. There is just impedance data, and the impedance varies with time. Hence, there is impedance vs. time data. The present invention provides that a waveform is obtained and the data is stored in a file. Post processing software is used to obtain the interconnect impedance versus time data (see, for example, the last couple sentence of the fourth paragraph of the "description" section of the application). In other words, impedance data is taken over a period of time, and this data is processed.

In the Office Action, the Examiner also rejected the claims citing United States Patent Nos. 6,605,954 (Nagar) and 6,191,601 (Swart) and United States Patent Application Publication No. US 2004/0217767 (DiOrio et al.). The claims have been replaced by new claims which further distinguish the claimed invention from that which is disclosed in the cited references. Applicant respectfully submits that what is now claimed is neither disclosed nor suggested by the prior art of record.

Two new independent claims have been added - claim 16 and 19. Claim 16 specifically claims a probe card which includes a package having solder balls mountable to a test head interphase board, and having electrically conductive material configured to electrically contact bumps on the device under test. Applicant respectfully submits that none of the cited references disclose or suggest providing such structure. While the Examiner has indicated that the Swart reference (U.S. Patent No. 6,191,601) does not disclose a probe card comprising solder balls on a first surface and an electrically conductive material on a second surface that is configured to electrically contact bumps on a substrate, the Examiner has taken the position that the DiOrio et al. reference (US Publication 2004/0217767) discloses wafer probing and particularly teaches "probe (see Fig. 2, interconnect substrate 220 and Fig. 3 probe card 330) comprising solder balls (222) on a first surface and an electrically conductive material on a second surface (340) that is configured to electrically contact bumps (112) on a substrate (350)."

Applicant respectfully traverses the Examiner's interpretation of DiOrio et al. In DiOrio et al., Fig. 2 is a conventional flip chip package (see paragraph 0020), in other words the device under test. Figure 2 does not illustrate a portion of the probe card. With regard to the probe card of DiOrio et al., DiOrio et al. merely discloses that the probe card has metal on pad (MOP) probes (340) for engaging contact terminals 114 of a device under test (see paragraph 0030). Applicant respectfully submits that the reference does not disclose or suggest providing a probe card which includes a package having solder balls mountable to a test head interphase board, and having electrically conductive material configured to electrically contact bumps on the device under test. As such, Applicant respectfully submits that claim 16 is allowable over Swart, DiOrio et al., or a combination of these references.

Claim 19, the other independent claim which has been added, is directed to a method, and specifically claims a step of providing a probe card such as that which is claimed in claim 16. Hence, Applicant respectfully submits that claim 19 is allowable for at least the same reasons that claim 16 is allowable. In addition, claim 19 specifically claims that the tester is configured to obtain a waveform from the DSO and store data in a file, and that the method includes the step of using post processing software to analyze the reflected signal and calculate interconnect impedance versus time data for the DUT. Applicant respectfully submits that this is not disclosed or suggested by the reference of record.

In view of the above amendments and remarks, Applicant respectfully submits that the claims of the application are allowable over the rejections of the Examiner. Should the present claims not be deemed adequate to effectively define the patentable subject matter, the Examiner is respectfully urged to call the undersigned attorney of record to discuss the claims in an effort to reach an agreement toward allowance of the present application.

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Respectfully submitted,

Date: March 21, 2005

By: _____

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